BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Sub B2 A1

1. (Amended) A method for making a thin film transistor containing a gate dielectric structure, comprising:

providing a substrate for the gate dielectric structure; and

providing an oxide layer of the gate dielectric structure on the substrate by an in-situ steam generation process.

Sub A2 B6

9. (Amended) A method for making a semiconductor device, comprising:

providing a substrate; and

providing a gate dielectric structure by:

providing a first oxide layer on the substrate by an in-situ steam generation process;

providing a nitride layer on the oxide layer; and

providing a second oxide layer on the nitride layer.

Sub A3 B8

24. (Amended) A SONOS semiconductor device made by the method comprising:

providing a substrate; and

providing a gate dielectric structure by:

providing a first oxide layer on the substrate by an in-situ steam generation process;

providing a nitride layer on the oxide layer; and

providing a second oxide layer on the nitride layer.

Sub A4 B10

26. (Amended) An integrated circuit containing a SONOS semiconductor device made by the method comprising:

providing a substrate; and

providing a gate dielectric structure by:

providing a first oxide layer on the substrate by an in-situ steam generation process;

providing a nitride layer on the oxide layer; and

providing a second oxide layer on the nitride layer.

Information Disclosure Statement

Applicants submitted an Information Disclosure Statement (IDS) to the Office on May 17, 2002. The Office did not reference the IDS in the Office action. Acknowledgement of the IDS is respectfully requested.

Claim Rejection – 35 U.S.C. § 102(e)

Claims 1, 3-7, 9-19, and 23-26 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Kusumi et al. (U.S. 2002/0039822 A1) for the reasons listed on pages 2-3 of the Office Action. Applicants respectfully traverse this rejection.

Independent claims 1, 9, 16, and 21-26 all containing the limitation that the oxide layer comprising the gate dielectric structure is made by an in-situ steam generation (ISSG) process. In one aspect of the invention, the ISSG oxide layer is part of the gate dielectric structure, e.g., in a SONOS device, it is the bottom oxide layer (25 in Figure 1) of the gate dielectric structure (25, 30, and 35 in Figure 1). In another aspect of the invention, the oxide layer can comprise all of the gate dielectric structure, e.g., in a TFT device, the oxide layer (56 in Figures 2a and 2b) is the gate dielectric structure. When the gate dielectric structure contains only an oxide layer, it is typically referred to as the "gate oxide" film (or layer).

The Office contends that Kusumi et al. disclose the limitations in these independent claims by providing an oxide layer 31b of the gate dielectric structure 36 on substrate 21 by an ISSG process, citing Figures 53-54H and paragraphs 0210 and 0528. Applicants disagree with this representation of the disclosure of Kusumi et al.

In the portions cited by the Office (i.e., the twelfth embodiment), Kusumi et al. describe the manufacture of a memory element. The preliminary steps for making this memory element are the same as those described in the first embodiment. *See* ¶ 0524 – 0526. These preliminary steps include forming the "gate oxide" film 28 by thermal oxidation of substrate 21. *See* ¶ 0161. Next, the polysilicon gate electrode 31A is formed on top of the gate oxide film 28. *See* ¶ 0167 – 0170 and 0527. Then, the layer 31b is formed by thermally oxidizing the polysilicon gate electrode 31A with water vapor to grow an oxide layer with a thickness of 5-15 nm on each of the side portions of the gate electrode 31A. *See* ¶ 0528.

In light of this disclosure of the twelfth embodiment, Kusumi et al. does not disclose forming the oxide layer of a gate dielectric structure using an ISSG process. The oxide 31b formed by the process of Kusumi et al. is not a gate oxide film. Rather, the oxide layer 28 is the gate oxide layer. The layer 31b is what is often referred to as a "sidewall" oxide because it is formed on the sidewall of the gate electrode.

The Office, therefore, has not substantiated that Kusumi et al. disclose that the gate oxide layer 28 is formed by an ISSG process. Thus, the Office has not shown that Kusumi et al. disclose each and every limitation in the present claims and, therefore, this rejection should be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 2, 8, and 20-22 have been rejected under 35 U.S.C. § 103 as being unpatentable over Kusumi et al. (U.S. 2002/0039822 A1) and Yu et al. (U.S. Patent No. 6,362,085) for the reasons listed on pages 3-4 of the Office Action. Applicants respectfully traverse this rejection.

The Office admits that Kusumi et al. does not disclose (1) a glass substrate and (2) annealing the oxide layer is a nitric oxide atmosphere. The Office argues that Yu et al. disclose such limitations and that it would have been obvious to combine the teachings of Yu et al. with Kusumi et al. because (1) glass substrates are well known in the art and (2) it would have increased the dielectric constant and improved the hot carrier hardness of the oxide layer.

Applicants respectfully disagree that the skilled artisan would have motivated to combined the cited references in the manner proposed by the Office. As to the first part of the Office's argument, just because it is well known in the art does not provide sufficient motivation. *See* M.P.E.P. § 2143.01, noting that modifications of prior art not *prima facie* obvious merely because aspect of the claimed invention was "well known" in the art.

As to the second part of the Office's argument, Yu et al. describe that it is desirable to incorporate nitrogen in the gate oxide to increase the dielectric and hot carrier resistance. *See* column 1, lines 49-54. Immediately after this description, however, Yu et al. describe that in "undesirable side effects were encountered" in incorporating the nitrogen into the gate oxide layer. *See* column 1, lines 54-57. Such undesirable side effects, however, would have discouraged—rather than encouraged—the skilled artisan to make the proposed modification.

Even if the Office's argument is true (an argument which Applicants do not agree with for the reasons above), it does substantiate that the combined teachings of Kusumi et al. and Yu et al. teach or suggest forming an oxide layer of a gate dielectric structure using an ISSG process. As noted above, Kusumi et al. do not teach forming the gate oxide layer 28 using an ISSG

process. And the Office has given no reason why the disclosure of Kusumi et al. would have suggested any modification to the skilled artisan. Further, the Office has not argued—much less alleged—that Yu et al. teach or suggest such a limitation.

Thus, the Office has not substantiated that the cited references, either alone or combined, teach or suggest forming the oxide layer of the gate dielectric structure using an ISSG process. Accordingly, the Office has failed to establish a *prima facie* case of obviousness and this rejection should be withdrawn.

CONCLUSION

For the above reasons, Applicants respectfully request the Office to withdraw these rejections and allow the pending claims.

If there is any fee due in connection with the filing of this Request for Reconsideration, please charge the fee to our Deposit Account No. 18-0013/40025-005.

Respectfully Submitted,

By _____
KENNETH E. HORTON
Reg. No. 39,481

Date: May 17, 2002